Amendments to the specification

Please replace the second whole paragraph on page 8 with the following amended paragraph.

After the checking patterns are formed on the four stacked semiconductor layers, overlap accuracy of the resulting target patterns on the four semiconductor layer is measured by overlay scanning. As FIG. 2D shows, the center position ~~Y0~~ of the first checking pattern 110 along the first dimension (i.e. Y-axis) is obtained and the center position ~~Y1~~ of the fourth checking pattern 440 along the Y-axis is also measured. When the difference between the center position of the first checking pattern 110 along the Y-axis ~~Y0~~ and ~~Y1~~ the center position of the fourth checking pattern 440 along the Y-axis is within a predetermined error range, the resulting target patterns on the fourth semiconductor layer align with those on the first semiconductor layer along the Y-axis.

Please replace the whole paragraph bridging pages 8 and 9 with the following amended paragraph.

Subsequently, the center positions of the second checking pattern and the third checking pattern are measured by overlap scanning. A first average position ~~X01~~ along the second dimension (i.e. X-axis) between the second checking pattern 220 and the third checking pattern 330 on one side is measured. A second average position ~~X02~~ between the second checking pattern 220 and the third checking pattern 330 on the other side is then measured. An average value of the first average position ~~X01~~ and the second average position ~~X02~~ is obtained to represent the center position

~~X0~~ of the second checking pattern 220 and the third checking pattern 330. Subsequently, the center position ~~X1~~ of the fourth checking pattern 440 along the X-axis is measured. When the difference between the center position of the second checking pattern 220 and the third checking pattern 330~~X0~~ and ~~X1~~ the center position of the fourth checking pattern 440 along the X-axis is measured is within a predetermined error range, the resulting target patterns on the fourth semiconductor layer align with those on the second and third semiconductor layers along the X-axis.

Please replace the paragraph bridging pages 10 and 11 with the following amended paragraph.

After the checking patterns are formed on the four stacked semiconductor layers, overlap accuracy of the resulting target patterns on the four semiconductor layer is measured by overlay scanning. As FIG. 3D shows, the center position ~~Y'0~~ of the first checking pattern 110 along the first dimension (i.e. Y-axis) is obtained and the center position ~~Y'1~~ of the fourth checking pattern 440 on the fourth semiconductor layer along the Y-axis is also measured. When the difference between the center position of the first checking pattern 110 ~~Y'0~~ and the center position of the fourth checking pattern 440~~Y'1~~ is within a predetermined error range, the resulting target patterns on the fourth semiconductor layer align with those on the first semiconductor layer along the Y-axis.

Please replace the first whole paragraph at page 11 with the following amended paragraph.

Subsequently, the center positions of the second checking pattern and the third checking pattern are measured by overlap scanning. The ~~position X'01 of the~~ second checking pattern 220 on one side of the second pair of parallel sides 520 and ~~the position X'02 of~~ the third checking pattern 330 on the other side of the second pair of parallel sides 520 are measured. A average value of ~~the position X'01 of~~ the second checking pattern 220 on one side of the second pair of parallel sides 520 and ~~the position X'02~~ the third checking pattern 330 on the other side of the second pair of parallel sides 520is obtained to represent the center position ~~X'0~~ of the second checking pattern 220 and the third checking pattern 330. Subsequently, the center position ~~X'1~~ of the fourth checking pattern 440 along the X-axis is measured. When the difference between the center position of the second checking pattern 220 and the third checking pattern 330~~X'0~~ and the center position of the fourth checking pattern 440 along the X-axis ~~X'1~~ is within a predetermined error range, the resulting target patterns on the fourth semiconductor layer align with those on the second and third semiconductor layers along the X-axis.

Please replace the first, second and third whole paragraphs on page 12 with the following three amended paragraphs.

FIG. 4C shows still another modification of the first embodiment in the present invention. The fourth checking pattern 440 is formed by exposing the fourth photomask on the fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 4C shows, the fourth photomask defines a second rectangle frame 600 as the fourth checking pattern 440 on the fourth semiconductor layer 400 and the first rectangular frame 500 is surrounded by the fourth checking pattern 440.

FIG. 4D shows one modification of the second embodiment in the present invention. The fourth checking pattern 440 is formed by exposing the fourth photomask on the fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 4D shows, the fourth photomask defines a second rectangular frame 600 as the fourth checking pattern 440 on the fourth semiconductor layer 400 and the first rectangular frame 500 is surrounded by the fourth checking pattern 440.

If the difference between the center position of the second checking pattern 220 and the third checking pattern 330 and the center position of the fourth checking pattern 440 along the X-axis ~~X0 and X1~~ and /or the difference between the center position of the first checking pattern 110 along the Y-axis and the center position of the fourth checking pattern 440 along the Y-axis ~~Y0 and Y1~~ are not within the corresponding predetermined error ranges, which means the target patterns on the fourth semiconductor layer misalign with those on the first, second

and/or third semiconductor layers, the patterns on the fourth semiconductor layer are removed and then re-exposed to form aligned patterns.